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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/783,598

02/15/2001

Kiyokazu Moriizumi

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EXAMINER

DINH, TUAN T

ART UNIT

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2841

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 09/783,598	<b>Applicant(s)</b> MORIIZUMI, KIYOKAZU	
	<b>Examiner</b> Tuan T. Dinh	<b>Art Unit</b> 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 13 May 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 and 3-16 is/are pending in the application.
- 4a) Of the above claim(s) 7-16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 and 3-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin et al. (U.S. Patent 5,916,453) in view of Albrecht et al. (U.S. Patent 4,968,585), and further in view of Ho et al. (U.S. Patent 5,354,712).

As to claim 1, Beilin et al. discloses (see column 6, lines 17-67) a front-and-back electrically conductive substrate as shown in figures 1-17, and in particular figure 9 comprising:

a plurality of posts (18 or 118) extending through the substrate, said post (18) formed of anisotropically etched (because column 6, line 17 states that the post is made by anisotropically etching (16) to form the post; therefore, the post is anisotropically etched). Each post has an electrically conductive portion (14) that has at least first and second surfaces (figures 7-9 show pads 14 connected on the top and bottom surfaces of the posts 18 for making electrical connection); and an insulative substrate (20).

Beilin et al. does not disclose the post (18) made from silicon; therefore, does not teach that the post being formed by etching silicon using anisotropical etching.

“[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

Reference Beilin discloses all the features of the claimed invention (said post (18) formed of anisotropically etched) except for process limitations. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same, or obvious over the prior art. See Product by process in MPEP §2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Albrecht et al. shows micro-miniature tips formed using semiconductor IC technique as shown in figures 1-5 comprising a Silicon (Si) post (18) being formed by anisotropically etched silicon, see abstract, lines 4-6, column 2, lines 30-37, column 3, lines 9-11, and column 4, lines 16-47).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the silicon post of Albrecht employed the post of Beilin in order to achieve a fine pitch interconnection applied in a high density interconnection of a wiring board or a multilayer substrate by using silicon as a dielectric allowing much more precision than some of the other materials.

Beilin and Albrecht do not specific disclose a side-face of the post being covered by an electrically conductive film so as to provide electrical contact between said one side and other side of the substrate.

Ho shows an interconnection structure as shown in figures 1a-1c comprising a side face of an interconnection (31) being covered by an electrically conductive film (22) so as to provide electrical contact between said one side and other side of a substrate (18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a side face of a post being covered by an electrically conductive film as taught by Ho employed in the substrate of Beilin and Albrecht in order to provide a protection barrier side surfaces for the post.

As to claim 3, Beilin as modified as above (see claim 1) discloses the insulative substrate (20) is composed of an organic resin (column 4, lines 10-35); and the electrically conductive portion (14) is a metal having a melting temperature higher than a melting temperature of an insulation used in the insulative substrate (20), (Note: the melting temperature of metal is higher than the melting temperature of the resin material of the insulative substrate, for example, copper (Cu) having the melting temperature higher than the melting temperature of resin (plastic or silicon et.)).

As to claim 5, Beilin as modified as above, as shown in figure 9, discloses a wiring pattern layer (the wiring is near the pad 14 formed on the top surface) and an insulation layer (another insulative layer 20 on top of the layer 20, see figure 9) is formed on at least the first surface (top surface) of the substrate.

3. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beilin et al. ('685) in view of Albrecht et al. (585) and Ho ('712), and further in view of Onishi et al. (U.S. Patent 5,459,368).

As to claim 4, Beilin and Albrecht et al. and Ho ('712) teach the substrate further comprising a pad (14). However, they do not specific disclose pad (14) for mounting a semiconductor component is formed on at least the first surface of the substrate.

Onishi et al. teaches an electronic device (1) as shown in figure 1 mounted on a pad of a substrate.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a pad for mounting a device, as taught by Onishi et al. employ in the substrate of Beilin and Albrecht et al. and Ho for the purpose of providing an excellent electrical connective bonding.

As to claim 6, Beilin and Albrecht et al., Ho ('712) do not teach the insulation material of the insulative substrate having compensation of CTE different from the CTE of a mounted semiconductor component. However, Onishi et al. show a surface acoustic wave device mounted module in figure 1 comprising a surface acoustic wave element (1) made of at least one material selected from a group consisting of lithium niobate, lithium tannalate, lithium borate, and quartz, and an insulating resin multiplayer substrate (8), see column 4, lines 36-47. There is a compensation of different material between the multiplayer substrate and the element that would have different CTE therebetween.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the compensation of a different material having different CTE in the substrate of Beilin and Albrecht et al. and Ho ('712), as taught by Onishi et al., for the purpose of providing the sufficient melting temperature that applied on a component when mounted on a substrate.

### ***Response to Arguments***

4. Applicant's arguments filed 10/31/07 have been fully considered but they are not persuasive.

Applicant argues:

a) The combination of Beilin and Albrecht fails because Beilin does not “teach or require anisotropically etching step.”

*Examiner disagrees. As in Beilin, the conductive post (18) formed by anisotropically etched (see noted as in claim 1) may be formed of other materials besides conductive material (see column 4, lines 15-16). The other material of the post's Beilin could be a silicon (Si). However, for the applicant benefit, Albrecht shows a silicon post made by etching silicon using anisotropically etched. Beilin and Albrecht are the same field. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the silicon post of Albrecht employed the post of Beilin in order to achieve a fine pitch interconnection applied in a high density interconnection of a wiring board or a multilayer substrate by using silicon as a dielectric allowing much more precision than some of the other materials.*

*Thus, the combination of Beilin and Albrecht meet the claimed invention.*

b) Beilin and Albrecht in view of Ho, specific of Ho does not disclose or teach “the post being made by etching.”

Examiner disagrees. Ho shows an interconnection structure as shown in figures 1a-1c comprising a silicon substrate (18) having side face of an interconnection (31) by etching process (see columns 6-7) and being covered by an electrically conductive film (22) so as to provide electrical contact between said one side and other side of a substrate (18). Even though Ho does not specific disclose the post form by etching step. However, the interconnected (31) is provided electrical contact from one to another side of the substrate, the interconnection can be act as a post. Thus, the combination is meets the claim.

### ***Conclusion***

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.



Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Dinh whose telephone number is 571-272-1929. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reichard Dean can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T Dinh/  
Primary Examiner, Art Unit 2841.